# Coupling Between Microstrip Lines With Finite Width Ground Plane Embedded in Thin-Film Circuits

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***Abstract*—Three-dimensional (3-D) interconnects built upon multiple layers of polyimide are required for constructing 3-D circuits on CMOS (low resistivity) Si wafers, GaAs, and ceramic substrates. Thin-film microstrip lines (TFMS) with finite-width ground planes embedded in the polyimide are often used. However, the closely spaced TFMS lines are susceptible to high levels of coupling, which degrades the circuit performance. In this paper, finite-difference time domain (FDTD) analysis and experimental measurements are used to demonstrate that the ground planes must be connected by via holes to reduce coupling in both the forward and backward directions. Furthermore, it is shown that coupled microstrip lines establish a slotline type mode between the two ground planes and a dielectric waveguide type mode, and that the connected via holes recommended here eliminate these two modes.**

***Index Terms*—Coupling, crosstalk, finite-difference time domain (FDTD), microstrip.**

## I. Introduction

DEMAND is growing for packaged microwave monolithic integrated circuits (MMICs) with greater functionality, lower cost, and smaller size. Furthermore, the digital processing and control functions of the system are now often incorporated into the same package as the analog circuits and MMICs. However, consumer, military, and aerospace components must fit into smaller areas. Thus, two-dimensional packages are no longer suitable for many of these applications. Instead, three-dimensional (3-D) packages and integration technologies are required.

A widely used, low-cost technology that is currently used for packaging individual circuits and integrated systems is low-temperature cofired ceramic (LTCC). By laminating multiple layers of thick (0.1–0.15 mm) ceramic sheets with thick-film metal lines on each layer and metal filled via holes to interconnect the various layers, complex 3-D circuits are possible [1]–[3]. An alternative multilayer packaging technology is commonly called multichip module-deposited (MCM-D) [4]–[6] or high-density interconnect (HDI) [7] that consists of multiple layers of thin-film polyimide deposited onto a ceramic carrier. Portions of a thin-film metal circuit are fabricated on each layer of polyimide and interconnected by etched via holes. MMICs and integrated circuits (ICs) may be attached to the upper polyimide layer after the final layer is deposited, or they may be placed in wells etched into the ceramic carrier. Instead of thin deposited polyimide layers on ceramic and flip-chip or wire bonded circuits, higher levels of integration and circuit variability are possible by depositing polyimide directly onto GaAs [8], [9] and Si [10], [11] substrates with all of the circuitry monolithically fabricated on the same wafer. In this way, passive circuit components, which occupy most of the area of ICs and MMICs, and antennas may be placed over the active circuits that are fabricated on the semiconductor. Thin-film polyimides on Si could possibly alleviate the problem that microwave passive elements and transmission lines placed directly on standard CMOS and BiCMOS grade Si, which have resistivities of 1 and 20 $\Omega-$cm, respectively, have low quality factors (high attenuation), which necessitates novel transmission line structures [12] that are typically embedded in the polyimide.

Achieving sufficient isolation between transmission lines embedded in multilayer substrates is critical for proper circuit/system performance. However, when transmission lines are close together, direct coupling between them is high, and in multilayer circuits where transmission lines may be under each other, the coupling is even higher [13]. In addition to direct coupling, transmission lines on isotropic and anisotropic substrates may excite surface waves on the substrate that will leak power away from the excited line and couple it to other lines on the substrate. It has also been shown that these leaky, surface wave modes may have an electromagnetic field distribution that resembles the field distribution of a microstrip line near the line [14]. Thus, it is easily excited in circuits.

A commonly used transmission line in these multilayer circuits and packages is microstrip or, as it is called when implemented on thin films, thin film microstrip (TFMS). When used on Si CMOS and BiCMOS circuits, it provides a low-loss transmission line since the ground plane shields the electromagnetic fields from the lossy Si [12]. The coupling between microstrip lines with infinite ground planes built on LTCC [15] and embedded in polyimide [16], [17] with shielding structures built into the substrate has been thoroughly characterized. However, in many of these 3-D circuits and packages, a finite-width ground plane is used to enable higher levels of integration, and on LTCC packages where a high percentage of the ceramic must be open to ensure ceramic bonding and control shrinkage, finite-width ground planes are required. TFMS with finite-width ground planes have a higher loss than conventional

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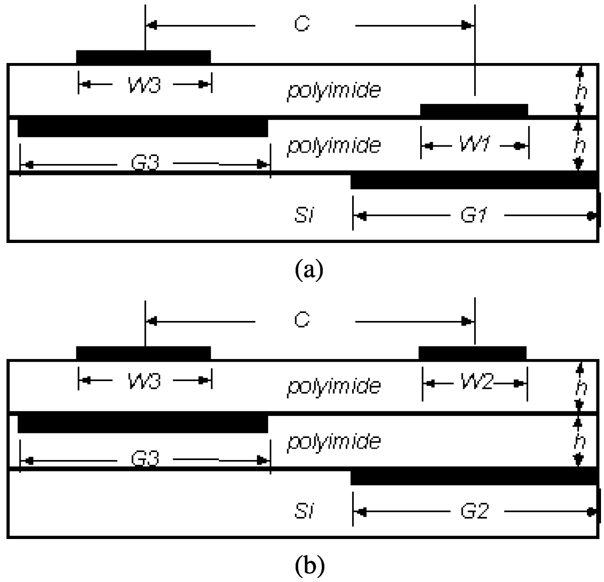


Fig. 1. Cross-sectional cuts through microstrip lines with finite width ground planes embedded in polyimide layers. (a) Microstrip lines with same substrate thickness. (b) Microstrip lines with different substrate thickness.

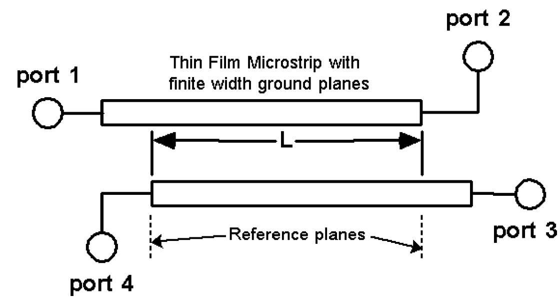


Fig. 2. Schematic of the four-port microstrip line structure used to characterize coupling experimentally. The same port designations used in the FDTD analysis.

microstrip lines, but, if the ground plane is greater than 3 to 5 times the strip width, acceptable attenuation is achieved [18]. Also, by reducing the ground plane width, ground planes may be placed on different layers to give another design option. For example, antenna radiation characteristics are modified by changing the ground plane dimensions of microstrip patch antennas [19]–[21].

Coupling between finite-width ground plane microstrip lines embedded in polyimide has been experimentally investigated [22]. However, [22] raised questions about parasitic modes that could not be answered experimentally. In this paper, an analysis of the coupling between TFMS lines with finite-width ground planes embedded in polyimide built upon CMOS grade Si is presented. This analysis includes a comparison of the coupling between transmission lines built on different layers of polyimide, and the use of metal filled via posts to connect ground planes on different layers. An emphasis is placed on a finite-difference time domain (FDTD) analysis of the lines to understand the parasitic modes and their role in the coupling characteristics. Also, the goal of this paper is to understand and propose methods to reduce unwanted coupling between two transmission lines that are parallel to each other for a short length and separate again, not to develop an understanding of couplers.

## II. Circuit Description

Fig. 1 shows a cross-sectional cut through two variations of microstrip lines embedded in polyimide upon a Si substrate. TFMS lines are characterized with ground plane widths of 3 and 5 times the strip width. W1, W2, and W3 are 23 $\mu$m, 52 $\mu$m, and 25 $\mu$m, respectively, to yield 50-$\Omega$ transmission lines for the polyimide thickness $h$ of 10 $\mu$m. Since the purpose here is to understand unwanted coupling between two microstrip lines that are parallel to each other and then separate again to interconnect circuit components, the ports are terminated in 50 $\Omega$. As was proposed in [22] and will be expanded upon here, there is an advantage to connecting the two ground planes. Thus, in several coupled microstrip lines and in the FDTD analysis, the two ground planes on different layers are connected by a single row of 20 by 20 $\mu$m via holes spaced 100 $\mu$m apart, which is a via spacing less than one hundredth of a wavelength at 25 GHz. To accomplish this when the ground planes did not overlap, the ground planes were extended in one direction so that they overlapped by 20 $\mu$m. The parameter $C$ is the distance between the centerlines of the two TFMS lines.

For the experimental characterization, a four-port circuit is used for measuring the coupling between the microstrip lines with probe pads oriented so that each port may be probed simultaneously with the port numbering as shown in Fig. 2. The 90° bends are not required for the FDTD analysis. The coupling region, or the section of parallel transmission lines labeled $L$ in Fig. 2, is 5000-$\mu$m-long for the experimental characterization, but the coupling length was varied from 3000 to 5000 $\mu$m for the FDTD analysis. While these are physically short lines, they have an electrical length between 180° and 270° at 25 GHz, which is required for rat-race, hybrid, and Wilkinson dividers. Longer lines, which would have higher coupling, would be required for antenna feed networks.

## III. Theoretical Analysis

The full-wave FDTD technique [23] is used for the theoretical characterization of the forward and backward coupling, $S_{31}$ and $S_{41}$, respectively, between the two parallel microstrip lines, which are assumed to be lossless for the numerical analysis. The E- and H-field components are implemented in a leapfrog configuration. An adaptive grid with neighboring cell aspect ratio smaller or equal to two maintains a second-order global accuracy.

Numerical 3-D meshes of 80–120 by 45 by 250 cells terminated with ten perfectly matched layer (PML) cells in each direction provide accurate results for a time-step of $\Delta t = 0.99\Delta t_{\max}$. A Gaussian pulse with $f_{\max} = 60$ GHz is applied vertically as a soft source close to the front end of the microstrip, and its values get superimposed on the FDTD calculated field value for all cells in the excitation region for each time-step. More details about the FDTD simulation are given in Section VII. The via holes are modeled as rectangular metal tubes with cross section 23 × 20 $\mu$m. To account for the excitation of different modes in the microstrip lines, two simulations are performed for each geometry, exciting both lines with equal amplitude and even or odd space distributions, respectively. In addition, both microstrip lines are terminated with matched loads ($Z_o = 50\ \Omega$) that are realized as the combination of shunt resistors placed between the microstrip and the bottom ground [24]. Probes placed at the front end and at the far end of one line are used for the combination of the results of the even and of the odd simulations. The application of the FFT algorithm derives the frequency-domain results from the time-domain data (usually 20 000 time-steps).

As will be shown in a later section, multiple modes propagate along the coupled line. Therefore, to assure that the microstrip mode characteristics are being measured, two probes, equally spaced to the left and right of the center of the microstrip line are used and the average of those two probe voltages yields the microstrip mode voltage.

## IV. Circuit Fabrication and Characterization

The four-port microstrip circuits are fabricated on a 1-$\Omega-$cm Si wafer. The lowest level ground plane consisting of a 300-Å Ti adhesion layer, 1.5 $\mu$m of Au, and a 200-Å Cr cap layer is first evaporated onto the Si wafer. Then, Dupont adhesion promoter and 10 $\mu$m of Dupont PI-2611 polyimide, which has a relative dielectric constant $\varepsilon_r$ of 3.12 measured at 1 MHz [25] and a loss tangent of 0.002 measured at 1 kHz [26], is spun onto the wafer. After curing the polyimide at 340 °C for 120 min, an Ni mask is evaporated and patterned on the polyimide for the $O_2/CF_4$ reactive ion etching (RIE) of the via holes. After the via holes are etched and the Ni removed, 200 Å of Ti and 2000 Å of Au are sputtered onto the wafer to serve as a seed layer for the 1.3 $\mu$m of Au electroplating that is used to define the embedded microstrip lines and fill the via holes in a single step. This Au is capped with 200 Å of Cr before applying the next layer of polyimide. Thus, all metal structures are 1.5-$\mu$m thick. This process is repeated for each layer of polyimide. A Dektak surface profile and an SEM analysis of the polyimide and metal strips show that the surface roughness is low enough that it can be neglected in the analysis.

Measurements are made on an HP8510C vector network analyzer from 1 to 50 GHz. A two-port thru/reflect/line (TRL) calibration is implemented with Multical [27], a TRL software program, using four delay lines of 1800, 2400, 4800, and 10 000 $\mu$m and a short circuit fabricated on the same substrate as the circuits. Each of these delay lines is straight, meaning that the two 90° bends shown in Fig. 2 are not de-embedded from the measurements. To improve accuracy, each circuit is measured several times and the average of those measurements is presented in this paper. Two of the four ports are terminated in 50-$\Omega$ loads built into especially designed RF probes during testing of the coupling circuits.

## V. Microstrip Characteristics

The measured effective permittivity $\varepsilon_{\text{eff}}$ and attenuation of the microstrip lines embedded in polyimide are shown in Fig. 3. It is seen that for $f < 40$ GHz, lines of width W1 and W3, which have nearly identical width, have similar attenuation, and the microstrip line with width W2, which uses the entire polyimide thickness for its substrate, has lower loss. However, above 40 GHz, the loss of the wider line on the thicker substrate is higher. FDTD simulations show that the magnitude of the electric fields excited into the silicon wafer from the edges of the ground planes increases with frequency. Furthermore, microstrip lines with thicker substrates, such as W2 [right line of Fig. 1(b)], have a larger penetration of electric fields in the silicon than lines on thinner substrates. Therefore, since the silicon is a lossy substrate, this is probably the reason for higher loss for line W2 at higher frequency. The effective permittivity of the completely embedded line, W1, is equal to the relative permittivity of the polyimide at high frequency.

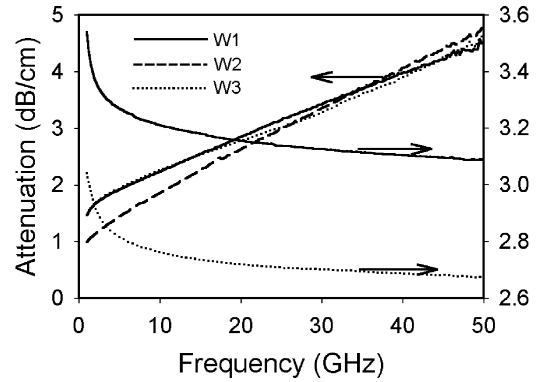


Fig. 3. Measured attenuation and effective permittivity of microstrip lines embedded in polyimide.

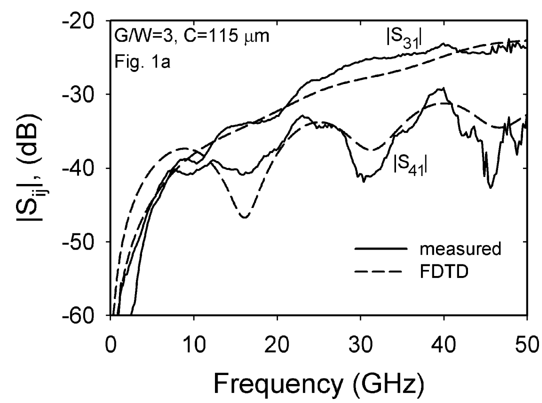


Fig. 4. Measured and FDTD analysis S-parameters for coupled microstrip lines with the same substrate thickness [Fig. 1(a)] and $L = 5000\ \mu$m as a function of frequency.

## VI. Microstrip Coupling

The measured and FDTD analysis results for the embedded microstrip lines are compared across the frequency band of 1 to 50 GHz for a typical case in Fig. 4. There is very good agreement with a maximum difference of 3 dB. Thus, conclusions from either technique may be assumed to be correct. Throughout the paper, the forward coupling is defined as $-20\log|S_{31}|$ and the backward coupling is $-20\log|S_{41}|$. Measured forward and backward coupling of TFMS lines is summarized in Fig. 5(a) and (b) respectively. It is seen that both forward and backward coupling decreases nearly linearly as $C$ increases, decreases by 3–5 dB as the ground plane increases from 3 to 5 W, and is 3–5 dB lower for the coupled TFMS of Fig. 1(a) compared to Fig. 1(b). Thus, to improve isolation, a wider ground plane and

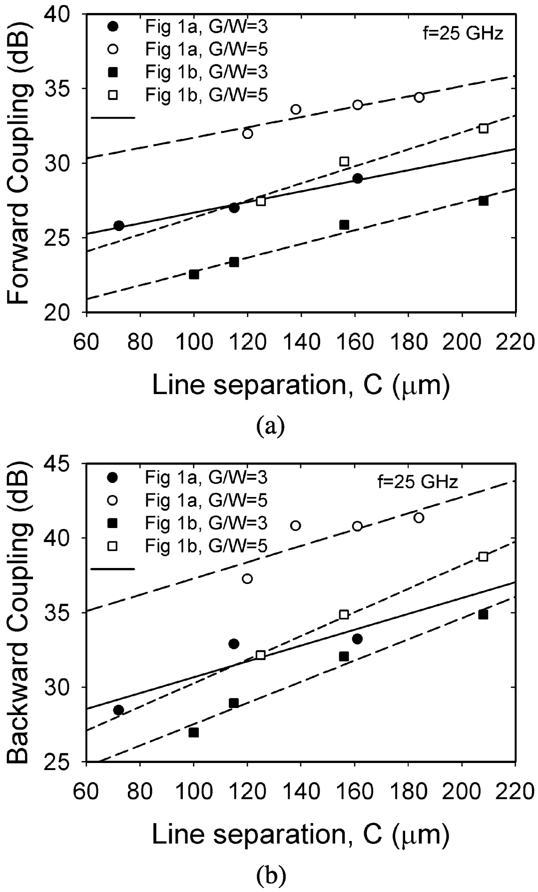


Fig. 5. Measured (a) forward and (b) backward coupling of coupled microstrip lines of Fig. 1(a) and (b) at 25 GHz and $L = 5000$ $\mu$m.

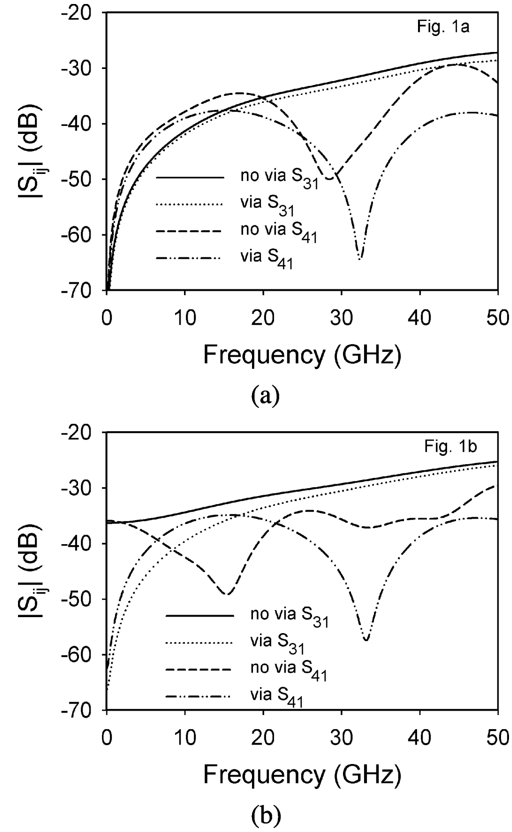


Fig. 6. FDTD analysis determined S-parameters for $C = 115$ $\mu$m, $L = 3000$ $\mu$m, and (a) structure of Fig. 1(a), and (b) structure of Fig. 1(b).

thinner microstrip substrates are desirable. Note that these results are for widely spaced transmission lines ($C/h{>}5$).

Returning to Fig. 4, it is noted that $|S_{31}|$ increases monotonically with frequency, but it does not increase as smoothly as the coupling between two typical TEM transmission lines [28] and coupled infinite-ground microstrip lines [17]. Backward coupling $|S_{41}|$ of two TEM transmission lines was expected to have a series of maxima of the same magnitude and a periodicity dependent on the coupling length $L$[29]. However, as seen in Fig. 4, $|S_{41}|$ has a periodic frequency dependence and a component that increases monotonically with frequency. Both of these characteristics is an indication that there are two components of coupling, direct coupling and indirect coupling through phantom circuits or, as they are now commonly called, parasitic modes [28]. This is not surprising because the coupled finite-width ground plane microstrip lines shown in Fig. 1 have four metal lines, which would support three independent TEM modes if the media were homogeneous. In addition, because the 3-D circuits consist of layers of low-permittivity material over the higher permittivity Si, slab waveguide/dielectric waveguide modes are possible. Thus, indirect coupling through phantom circuits is expected. A further cause of the ripples in $|S_{31}|$ and $|S_{41}|$ is that each mode has its own characteristic impedance, which differs from the 50-$\Omega$ termination impedance. Therefore, standing waves will be established between the input and output of the coupled line section. Also, the coupled line section supports an even and an odd mode, which will not have a 50-$\Omega$ characteristic impedance. It has been reported that terminating the even and odd modes will eliminate the ripples in $|S_{31}|$ and $|S_{41}|$ [30], [31], but with dielectric waveguide type modes and a third metal strip supported mode, it is not practical to terminate all of the modes. Thus, the standing waves of each mode will cause ripples in the coupling characteristics.

To reduce the number of modes, the two ground planes may be connected with via holes. It may be surmised that a coupled strip or slotline type mode propagates along the two coupled ground planes, and this mode is shorted by the metal interconnects. In [22], it was experimentally shown that connecting the two ground planes reduces coupling by 5 dB for a 5000-$\mu$m-long coupled line section. This conclusion is opposite to the case of coupled coplanar waveguides, where it has been shown that coupling is reduced if the ground planes between the two lines are separated by a gap as small as a few micrometers [32]. FDTD analysis of 3000-$\mu$m-long coupled lines, which is shown in Fig. 6, shows that the via posts reduces the effects of the parasitic modes. Note that $|S_{41}|$ is now periodic with frequency and $|S_{31}|$ increases smoothly with frequency for both cases [Fig. 1(a) and Fig. 1(b)].

## VII. Electromagnetic Fields of Coupled Lines

While the measured and the simulated coupling characteristics, $|S_{31}|$ and $|S_{41}|$, support conclusions that connecting the ground planes of microstrip lines greatly decreases coupling and eliminates or reduces the magnitude of parasitic modes, this conclusion needs further investigation. FDTD analysis is capable of mapping the electric and magnetic fields of coupled

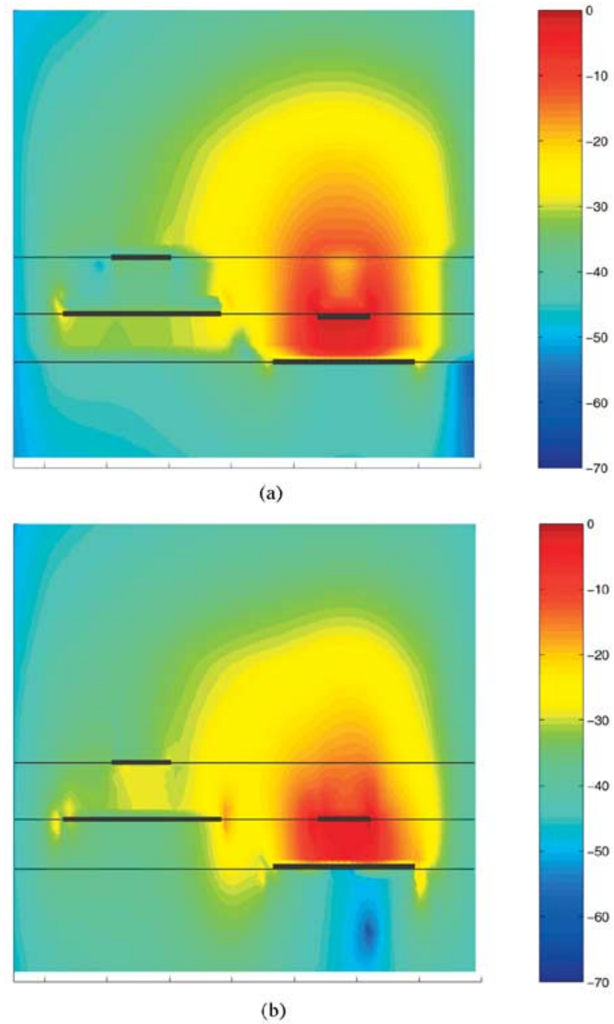


Fig. 7. FDTD derived (a) electric and (b) magnetic field plots for coupled microstrip lines shown in Fig. 1(a) without via posts at 20 GHz and $C = 92\ \mu$m. (Left-hand microstrip line width is W3 $= 23\ \mu$m and G3 $= 75\ \mu$m; right-hand microstrip line width is W1 $= 23\ \mu$m and G1 $= 69\mu$m. There is a 20-$\mu$m gap between the two ground planes).

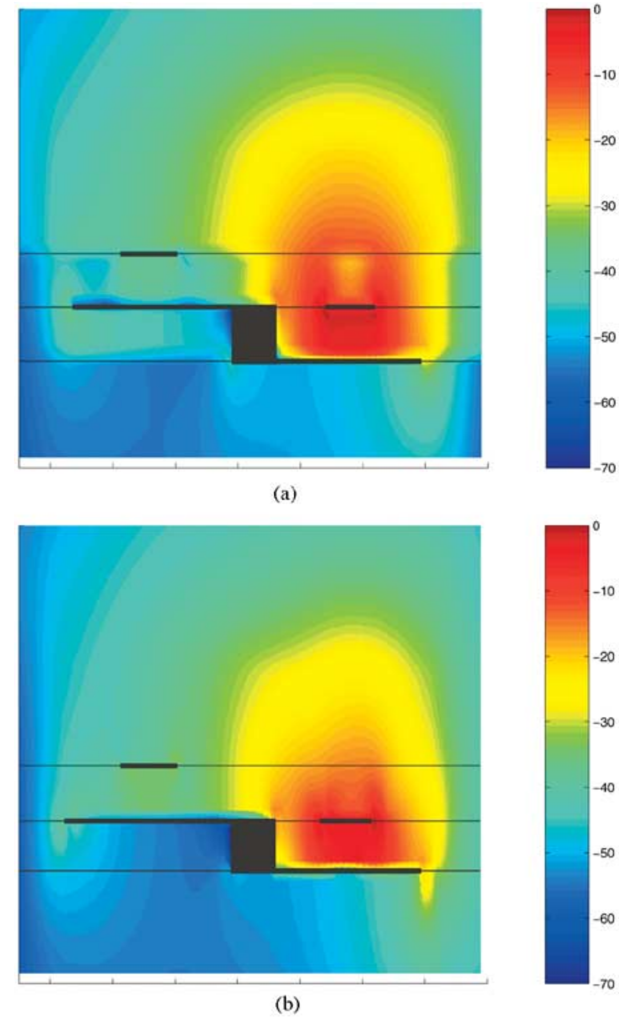


Fig. 8. FDTD derived (a) electric and (b) magnetic field plots for coupled microstrip lines shown in Fig. 1(a) with via posts at 20 GHz and $C = 92\ \mu$m. (The microstrip line dimensions are the same as in Fig. 7).

microstrip lines and separating them into the various modes by using cross-sectional probes for specific frequencies and identifying the differentiating features of the different modes. Figs. 7–10 show the electric and magnetic fields for two cases of coupled lines shown in Fig. 1 both with and without via posts. The electric fields for the lines without via posts shown in Figs. 7(a) and 9(a) show high fields between the ground plane and silicon substrate of the coupled line. Similarly, Figs. 7(b) and 9(b) show there are high magnetic fields between the ground planes of two microstrip lines. Lastly, the electric fields under the coupled line and between the ground planes are stronger for the coupled lines shown in Fig. 1(b). With the via posts, the fields between the two ground planes are completely eliminated, and the electric field under the ground plane of the coupled line is reduced. The effect is more prominent for larger spacing $C$ between the lines ($C = 115\ \mu$m versus $C = 92\ \mu$m) that allows for the easier excitation of the slotline mode between the grounds. These qualitative observations indicate two parasitic modes: the first is a dielectric waveguide type mode and the second is a slotline type mode between the two ground planes. The via posts reduce or eliminate both of these modes.

The field plots and the conclusions derived from them indicate the elimination of two parasitic modes. To confirm the existence of these modes and the effect of the via posts, the effective permittivity and magnitude of the electric field at 25 GHz at locations shown in Fig. 11 are calculated and shown in Table I. Four 2.5D-FDTD simulations were run for each geometry in order to calculate the cross-sectional field distribution of the four dominant modes: the exciting (wanted) microstrip mode, the coupled (unwanted) microstrip mode, the slotline mode between the left ground and the right signal line, and the dielectric waveguide mode under the left ground plane. To derive these mode patterns, the grid excitation was modified. The first two mode patterns were computed using a vertical E-field excitation between the respective signal and ground planes, the third one using a horizontal E-field excitation between the two metals and the last one using a vertical E-field excitation between the left ground plane and the dielectric interface. Choosing a $\beta$ value around 100–500 and assuming all four modes are quasi-TEM (something that is verified by simulations for five different $\beta$

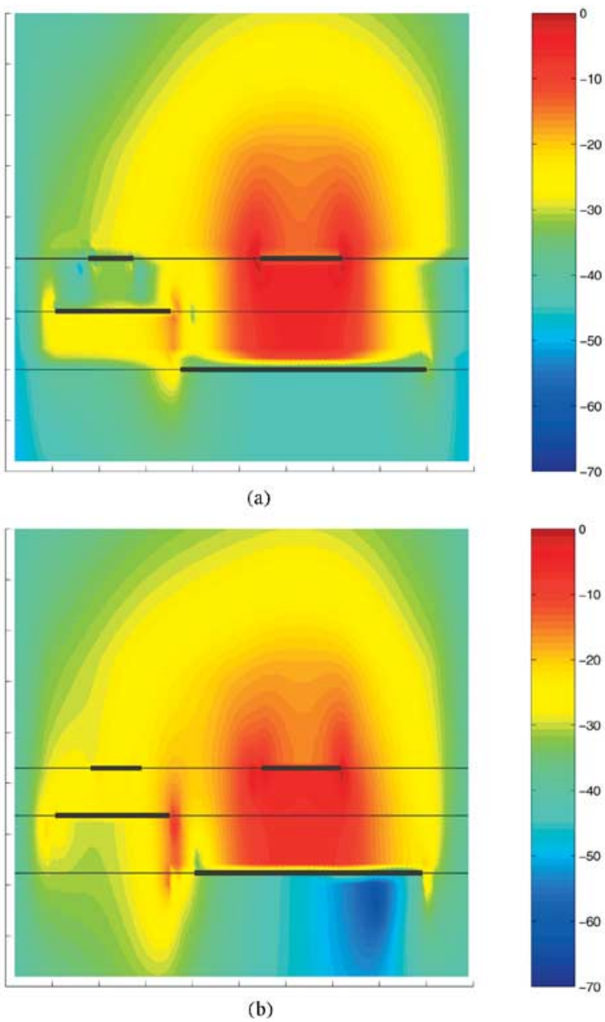


Fig. 9. FDTD derived (a) electric and (b) magnetic field plots for coupled microstrip lines shown in Fig. 1(b) without via posts at 20 GHz and $C = 115\ \mu$m. (Left-hand microstrip line width is W3 $= 23\ \mu$m and G3 $= 75\ \mu$m; right-hand microstrip line width is W2 $= 52\ \mu$m and G2 $= 156\ \mu$m. There is no gap between the two ground planes).

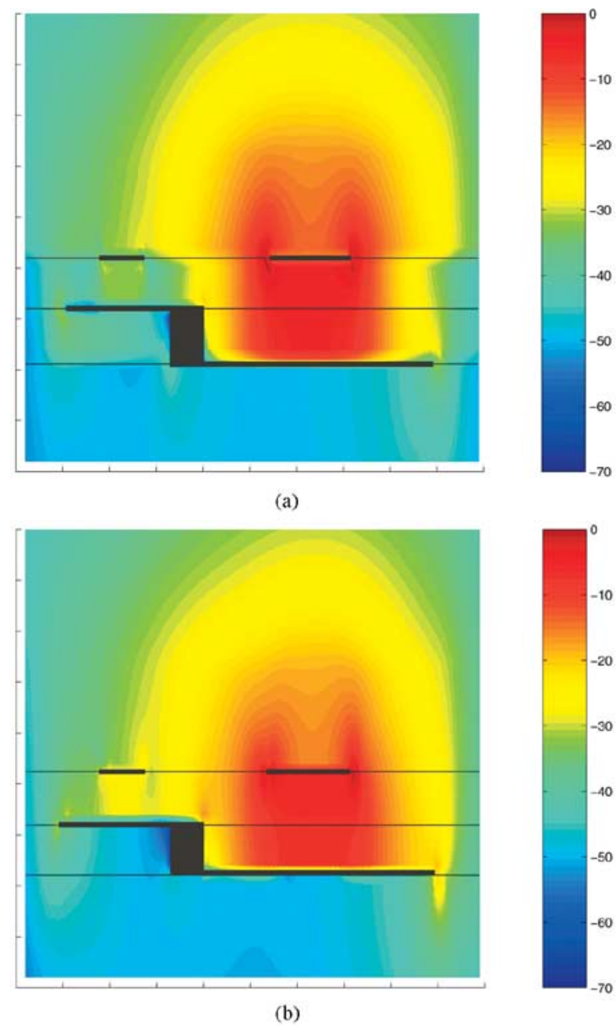


Fig. 10. FDTD derived (a) electric and (b) magnetic field plots for coupled microstrip lines shown in Fig. 1(b) with via posts at 20 GHz and $C = 115\ \mu$m. (The microstrip dimensions are the same as in Fig. 9).

values), the value of $\varepsilon_{\mathrm{eff}}$ can be easily determined by $\beta = 2\pi f(\mu_0\varepsilon_0\varepsilon_{\mathrm{eff}})^{0.5}$, where $f$ is the frequency derived by the maximum value of the probed field after FFT transform. The final step of mode separation involves two 3-D simulations, one for even and the other for odd excitation of both microstrip modes, something necessary considering the different phase velocities of these two spatial excitations. The four probes (1–4 in Fig. 11) are chosen appropriately close to the maximum field values of the above four modes. Integrating the cross-sectional total field values with the normalized mode distributions, derived from 2.5D-FDTD, leads to the amplitudes of the decomposed modes. The first conclusion of the simulations is that, qualitatively, the $\varepsilon_{\mathrm{eff}}$ of microstrip lines W1 and W3 shown in Table I agree with the measured values shown in Fig. 3. The FDTD analysis did not account for metal loss and, therefore, the effects of internal inductance on $\varepsilon_{\mathrm{eff}}$ are not included. Thus, a quantitative agreement cannot be obtained. Second, the addition of via posts does not change the $\varepsilon_{\mathrm{eff}}$ of the two microstrip modes, which indicates that the microstrip modes are not affected by the via posts. The 3-dB reduction in magnitude of the electric field for probe 2, the

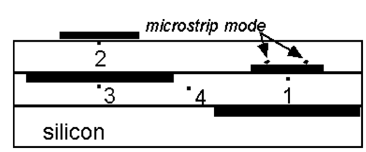


Fig. 11. Probe locations for determination of coupled microstrip modes. Probes 1 and 2 are the average of two probes spaced equal distant from center of line as shown above right-hand side microstrip. Probe 4 is equal distance between the left and right microstrip lines. Probe 3 is directly under the ground plane of the left line.

microstrip mode of the coupled line, with via post is a measure of the reduction in coupling that was presented in Fig. 6(a). The mode detected by probe 3 has an $\varepsilon_{\mathrm{eff}}$ greater than the $\varepsilon_{\mathrm{r}}$ of the polyimide, which indicates a mode that propagates in the silicon wafer and the polyimide below the ground plane. The via post reduces the magnitude of this mode by approximately 10 dB. In addition, the higher value of its $\varepsilon_{\mathrm{eff}}$ for the via-enabled geometry indicates that in this case, most of this mode is eliminated from the via-shielded lower $\varepsilon_{\mathrm{r}}$ polyimide and is concentrated in the silicon substrate. Because the $\varepsilon_{\mathrm{eff}}$ measured by probe 4 is nearly equal to the $\varepsilon_{\mathrm{r}}$ of the polyimide, it is surmised that this is

TABLE I
EFFECTIVE PERMITTIVITY AND MAGNITUDE OF MODES MEASURED AT PROBE POINTS SHOWN IN FIG. 11

| Probe and mode type | Effective permittivity | | Magnitude (dB) | |
|---|---|---|---|---|
| | No via | Via post | No via post | Via post |
| 1, microstrip (W1) | 2.89 | 2.90 | 0 | 0 |
| 2, microstrip (W3) | 2.73 | 2.70 | -27.5 | -30.2 |
| 3, dielectric waveguide | 4.54 | 6.93 | -31.2 | -42.0 |
| 4, slotline | 2.92 | - | -19.7 | - |

a slotline type mode between the two ground planes. This conclusion is supported by the elimination of this mode when the two ground planes are connected by via posts. However, without the via posts, this slotline mode is stronger than the microstrip mode in the coupled microstrip line. Other modes have magnitudes too small to influence the characteristics.

## VIII. CONCLUSION

In this paper, theoretical analysis and measured characteristics show that parallel, thin-film microstrip lines with finite-width ground planes support and excite multiple modes, which degrade the isolation between the lines. By interconnecting the two ground planes with equally spaced via posts, two of these parasitic modes are reduced or eliminated. One of the modes is a dielectric waveguide type mode that the via posts reduce by 10 dB. The other is a slotline type mode that is very strongly excited between the coupled lines without via posts. These results show that if finite-width ground plane microstrip lines are used for 3D-MMICs and thin-film packages, it is advisable to connect the ground planes periodically with metal-filled via posts and to use a wider ground plane width for higher isolation. Although these conclusions are based on experimental and theoretical analysis of thin film polyimide layers on silicon, they may be extended to other 3-D circuits and packaging structures that include multiple materials.

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